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5   S P E C I F I C A T I O N

HIGH-SENSITIVITY STORAGE PIXEL SENSOR
HAVING AUTO-EXPOSURE DETECTION

10   BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to digital cameras employing solid-state pixel

sensors. More particularly, the present invention relates to improved sensitivity and auto-

exposure detection apparatus and methods for use in digital cameras.

15   2. The Prior Art

Storage pixel sensors are known in the art. These devices sense photo-integrated

charge stored on a capacitor. A limitation of these prior pixels storage sensors is the

tradeoff that results from the desire for the capacitor to be small to achieve high

sensitivity and the competing desire for the capacitor to be large to provide low noise

20   and good storage time.

Prior art exposure control techniques known to the inventors that use the actual

image sensors during the actual exposure interval are of two types. Some prior art

techniques integrate the total photocurrent by a common back-side electrode (anode) of a group of photodiodes--i.e., they integrate the substrate current to get an average light reading on the whole array. Other prior art techniques use nondestructive readout to sample selected pixels during the exposure interval, looking for an indication that some

5   pixels are reaching a full-scale exposure. Another prior-art technique senses a total overflow charge from the pixel sensors.

The first technique is tricky and difficult to implement, since the photocurrents are small and the substrate is large and noisy. In addition, it responds strictly to the average

10   light level across the image plane rather than to those pixels that are reaching a full-scale charge accumulation. The second technique requires a sequential polling, so is limited to either a very slow operation or to sensing only a very small subset of the pixels. The second technique is therefore not good for detecting the exact time when a small percentage of pixels are reaching a full-scale exposure. The third technique requires

15   sensing of charges against a background of the total leakage of the full area of pixel sensors.

Other prior art techniques for exposure control typically measure the light either at a different time, e.g. just before the actual exposure, or with a different sensor device that needs to be calibrated relative to the sensor that is picking up the actual image. Such techniques typically sample the image plane at selected fixed points rather than adapting

5 to the lighting conditions of the entire image.

One such prior art technique uses an imager first to estimate a light level and thereby to calculate an optimum exposure duration for a second cycle of the imager. This technique is obviously not as fast, and particularly is unsuited to controlling the exposure

10 time rapidly during a dynamic lighting event, provided for example from a strobe flash.

Another such prior art technique employs a separate overall light sensor to measure an average light level and to react to a sufficient quantity of light by closing a shutter or quenching a strobe flash. Mechanical shutters and non-frame-storage

15 electronic sensors cannot be shuttered rapidly enough to use this technique during a flash, which is why the detector is sometimes used to turn off the light source instead of closing a shutter. These techniques require an awkward coordination between the camera, the

light sensor, and the light source, and do not necessarily track automatically the

sensitivity (or film speed) and lens aperture of the camera.

Another type of prior art technique relates to use of an adjustable overflow drain

5   for dynamic range enhancement. These techniques have not been integrated with the use

of the overflow current for terminating the exposure time. Variations on this technique

employ either a moving overflow barrier or a dual exposure interval to increase dynamic

range.

10   BRIEF DESCRIPTION OF THE INVENTION

According to a first aspect of the present invention, a MOS active storage pixel

sensor disposed on a semiconductor substrate comprises a photodiode having a first ·

terminal coupled to a first potential (ground) and a second terminal. A barrier transistor

has a first terminal coupled to the second terminal of the photodiode and a second

15   terminal coupled to a photocharge integration node comprising the control element of a

first source-follower transistor. A semiconductor reset switch has a first terminal coupled

to the second terminal of the barrier transistor and a second terminal coupled to a reset

reference potential that reverse biases the photodiode. The first source-follower transistor

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is coupled to a bias current source and has an output. A bias transistor has its drain

coupled to the output of the first source-follower transistor, its gate coupled to a fixed

potential to establish the saturation level along with the fixed voltage on the gate of the

saturation level transistor and a source coupled to a fixed voltage such as ground. A

5   semiconductor transfer transistor has a first terminal coupled to the output of the first

source-follower transistor and a second terminal connected to a capacitive storage node

comprising the control element of a second source-follower transistor having an output.

A row-select transistor has a first terminal coupled to the output of the second source-

follower transistor, a second main terminal coupled to a column output line and a control

10   element coupled to a row-select line. The reset transistor and the transfer transistor each

have a control element coupled to a control circuit for selectively activating the reset

transistor and the transfer transistor.

The separation of the photodiode from the charge integration node by the barrier

15   transistor allows high sensitivity, and the separation of the storage node from the charge

integration node by the first source-follower transistor allows low noise storage and

readout by providing a smaller capacitance for the charge integration node and a larger

capacitance for the storage node.

According to a second aspect of the present invention an auto-exposure circuit for use with pixel sensors is disclosed. A saturation level transistor has its source coupled to the output of the first source-follower amplifier, its gate coupled to a fixed potential

5   chosen to turn the transistor on at a preselected pixel voltage representing a saturation level, and a common (global) current summing drain node. A bias transistor has its drain coupled to the output of the first source-follower amplifier, its gate coupled to a fixed potential to establish the saturation current and a source coupled to a fixed voltage such as ground. The global current summing node is coupled to a current comparator to

10 compare the current flowing from the common drain node with a reference current. When the current from the global drain node exceeds the reference current, indicating that a preselected number of pixels in the array have saturated, the output of the comparator produces a TERMINATE EXPOSURE signal.

15   <u>BRIEF DESCRIPTION OF THE DRAWING FIGURES</u>

FIG. 1 is a schematic diagram of an illustrative MOS active pixel sensor incorporating an auto-exposure sensing circuit according to the present invention.

FIGS. 2A and 2B are timing diagrams that illustrate the operation of the pixel

sensor of FIG. 1.

FIG. 3 is a block diagram of an illustrative array of MOS active pixel sensors and

5   auto-exposure apparatus according to the present invention.

FIG. 4 is a diagram of an electronic camera including an array of pixel sensors and

auto-exposure apparatus according to the present invention.

10   <u>DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT</u>

Persons of ordinary skill in the art will realize that the following description of the

present invention is illustrative only and not in any way limiting. Other embodiments of

the invention will readily suggest themselves to such skilled persons having the benefit of

this disclosure. For example, the illustrative embodiments of the present invention are

15   disclosed using all N-Channel MOS transistor switches, but persons of ordinary skill in

the art will appreciate that other technologies could be employed as well. Such skilled

persons will readily understand how to adjust the polarities of the various potentials

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applied to the circuits disclosed herein to implement an embodiment of the present

invention employing such other technologies.

5   The present invention encompasses various combinations of elements in storage

pixel sensors. Different embodiments of storage pixel sensors according the present

invention include one or more of the following elements in combination incorporated into

the pixel sensor: a barrier transistor, a bias transistor for the source-follower transistor, a

saturation level transistor, and a transfer transistor. The present invention is disclosed

herein with reference to FIG. 1 as an embodiment including all of these elements in

10   combination with disclosure of how each element functions in the combination, but

persons of ordinary skill in the art will appreciate that multiple embodiments of the

invention are contemplated having one or more of these elements in combination in a

storage pixel sensor.

15   Referring first to FIG. 1, a schematic diagram of an illustrative high-sensitivity

pixel sensor 10 incorporating an auto-exposure control according to the present invention

is presented. Photodiode 12 has its anode coupled to a source of fixed potential (shown

as ground) and a cathode. The cathode of photodiode 12 is coupled to the source of MOS

N-Channel barrier transistor 14. The gate of MOS N-Channel barrier transistor 14 is coupled to a BARRIER line upon which a BARRIER control potential may be placed.

Persons of ordinary skill in the art will appreciate that the use of MOS N-Channel barrier transistor 14 is optional in storage pixel sensor 10 of the present invention, at the cost of

5   some sensitivity. Independent of the other transistors in the circuit, a barrier transistor 14 can be added to increase the sensitivity (the charge-to-voltage conversion gain) in darker areas of the image. The MOS N-Channel barrier transistor 14 allows essentially all of the charge from the photodiode to charge the gate capacitance of the first source follower transistor 20, providing a high gain, until that gate voltage falls low enough to turn the

10   barrier transistor 14 on more, after which the storage pixel sensor 10 operates in the lower-gain mode (for lighter areas) in which the charge is charging both the photodiode capacitance and the gate capacitance.

The cathode of photodiode 12 is coupled to a photocharge integration node 16

15   (represented in FIG. 1 as a dashed line capacitor) through the MOS N-Channel barrier transistor 14. A MOS N-Channel reset transistor 18 has its source coupled to the photocharge integration node 16, its gate coupled to a RESET line upon which a RESET signal may be asserted, and its drain coupled to a reset potential VR.

The photocharge integration node 16 comprises the inherent gate capacitance of

first MOS N-Channel source-follower transistor 20, having a drain connected to a voltage

potential VSFD1. The voltage potential VSFD1 may be held fixed at a supply voltage

5   V+ (which may be, for example, about 3-5 volts depending on the technology) or may be

pulsed as will be disclosed further herein. The source of MOS N-Channel source-

follower transistor 20 forms the output node 22 of the source-follower transistor and is

coupled to the drain of MOS N-Channel bias transistor 24 operating as a current source.

The source of MOS N-Channel bias transistor 24 is coupled to a fixed voltage potential

10   such as ground. The gate of MOS N-Channel source-follower bias transistor 24 is

connected to a bias voltage node. The voltage presented to the bias voltage node sets the

bias current flowing through MOS N-Channel source-follower bias transistor 24. This

voltage may be fixed, or, as will be disclosed further herein, may be pulsed to conserve

power. The use of MOS N-Channel source-follower bias transistor 24 is optional in the

15   present invention. As will be disclosed herein, this device is used in combination with a

saturation level transistor to implement an auto-exposure detection function.

The output node 22 of the source-follower transistor is coupled to a capacitive

storage node 26 (represented in FIG. 1 as a dashed line capacitor). In some embodiments

of the present invention, the output node 22 of the source-follower transistor is coupled to

the capacitive storage node 26 through a MOS N-Channel transfer transistor 28. The gate

5   of MOS N-Channel transfer transistor 28 is coupled to a XFR line upon which a XFR

signal may be asserted. MOS N-Channel transfer transistor 28 is an optional element in

the storage pixel sensor of the present invention.

The capacitive storage node 26 comprises the inherent gate capacitance of second

10   MOS N-Channel source-follower transistor 30, having a drain connected to a source-

follower-drain (SFD) potential and a source. The source of second MOS N-Channel

source-follower transistor 30 is coupled to COLUMN OUTPUT line 32 through MOS N-

Channel row select transistor 34. The gate of MOS N-Channel row select transistor 34 is

coupled to a ROW SELECT line 36.

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Second MOS N-Channel source-follower transistor 30 is preferably a large device,

having its gate sized at 10 to 100 times the area of first MOS N-Channel source-follower

transistor 20. The other transistors in the circuit, first MOS N-Channel source-follower

transistor 20, are preferably sized to near minimum length and width.

5　　　Use of a bias transistor 24 in the storage pixel sensor of the present invention can

change the operating characteristics of the pixel sensor in a beneficial way. The first

source-follower is working against a controlled current source, which may be more well

controlled than when working against only the capacitive load of the storage node

capacitance of the second source follower transistor 30.

10　　　To increase the input-to-output voltage gain of either source follower transistor 20

or 30, it is possible to pulse its drain terminal (as disclosed in FOV-013 for the readout

follower). If the drain of the first source follower transistor 20 is pulsed, current will

flow only when it is high, so the pixel saturation disclosed with reference to auto-

exposure circuit 40 can be monitored only while it is high. It may be advantageous to

15　　pulse drain of the first source follower transistor 20 with a low duty cycle to save power

during exposure. Pulsing drain of the first source follower transistor 20 also keeps the

photodiode and barrier source/drain voltages lower during the time the drain is low,

which can beneficially reduce voltage-dependent leakage at those nodes. If the

BARRIER and VR voltages are adjusted for proper barrier operation with the drain low,

then the barrier transistor 14 will tend to turn off while the drain of the first source

follower transistor 20 is pulsed, so the charge on the photodiode 12 will not be disturbed.

The exposure needs to end with the drain high to capture the final state on the storage

5   node.

Referring now to FIG. 2A, a timing diagram illustrates the operation of pixel

sensor 10 of FIG. 1. Initially, the RESET signal is asserted high. The VR node at the

drain of the MOS N-Channel reset transistor 18 is brought from zero volts to the voltage

10   VR. This action resets all pixel sensors in the array by placing the voltage potential VR

(less a threshold of the MOS N-Channel barrier transistor 14) at the cathode of each

photodiode 12. According to a presently preferred method for operating the high-

sensitivity pixel sensor of the present invention illustrated in FIG. 2A, the voltage VR is

initially at a low level (e.g., to zero volts) while RESET is high to reset the cathode

15   voltages of all photodiodes in the array to a low value to quickly equalize their states to

prevent image lag. Then the voltage VR is raised (e.g., to about 2 volts) for a

predetermined time (preferably on the order of a few milliseconds) while the RESET

signal is still asserted to allow the photodiodes in all pixel sensors to charge up to about

1.4 volts through their associated MOS N-Channel barrier transistors 14, whose gates are

held at about 2 volts. The black level at the integration node is thus set to VR, less a little

for the capacitive turn-off transient from the MOS N-Channel reset transistor, and the

photodiodes are reset to their respective appropriate levels as determined by their

5   respective barrier transistor thresholds. An advantage of this method is that those

thresholds don't affect the black level that is read out. After reset ends and integration

starts, some charge will still leak across the barrier by subthreshold conduction, but it

should be about the same for all pixels, or at least be a monotonic function of light level.

10   According to a particularly advantageous operation of the storage pixels sensor of

the present invention, the barrier transistor 14 and the reset transistor 18 are identically

sized so as to exhibit identical voltage thrsholds (Vth). The active level of the RESET

signal is chosen such that VRESET < VR + Vth, to achieve better tracking of

nonlinearities.

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When the RESET signal is de-asserted and photointegration begins, charge

accumulates on the photocharge integration node 16. Because MOS N-Channel barrier

transistor 14 is barely conducting, photoinduced charge trickles across its channel and

charges photocharge integration node 16 (by lowering its voltage) without lowering the

voltage on the cathode of the photodiode 12. This is advantageous because it minimizes

the capacitance charged by the photocurrent, thereby maximizing the sensitivity (volts

per photon).

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Persons of ordinary skill in the art will appreciate that the MOS N-Channel reset

transistor 18 can be coupled directly to the cathode of the photodiode 12, but such an

arrangement requires that the voltage VR be set precisely relative to the barrier voltage

and threshold. This is not preferred since the thresholds can vary.

10

The voltage at the source of first MOS N-Channel source-follower transistor 20,

and hence its output node 22, follows the voltage on its gate (the photocharge integration

node 16). In embodiments of the present invention that employ MOS N-Channel transfer

transistor 28, the XFR signal is asserted throughout the reset period and the integration

15   period and is de-asserted to end the integration period as illustrated in FIG. 2A. The low

level of the XFR signal is preferrably set to zero or a slightly negative voltage, such as

about -0.2 volts, to thoroughly turn off transfer transistor 28.

Ins. A To read out a pixel sensor, the SFD node at the drain of the second MOS N-

Channel source-follower transistor (labeled VSD2 in FIG. 2A) is driven to the voltage

VSFD, the ROW SELECT signal for the row of the array containing the pixel sensor 10

is asserted, and the output signal is thereby driven onto COLUMN OUTPUT line 32.

5   The timing of the assertion of the VSFD2 signal is not critical, except that it should

remain high until after the ROW SELECT signal is de-asserted as illustrated in FIG. 2A.

It may be advantageous to limit the voltage slope at the rising edge of the ROW SELECT

signal if VSFD2 is rasied first, as disclosed in co-pending application serial No.

_____, filed February 14, 2000, docket No. FOV-038.

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        Referring now to FIG. 2B, if the XFR transistor is not present, the storage node

may be isolated by lowering SFBIAS (preferably to zero or a slightly negative voltage

such as about -0.2 volts) and setting VR low, and then asserting the RESET signal. This

sequence turns off the first source follower 20 by lowering the voltage on its gate while

15   its load current is turned off, thereby storing its output voltage.

        In FIG. 2B, the VR falling edge and the RESET rising edge are shown following

closely on the terminate signal, since these transistors isolate the storage node to end the

exposure. In FIG. 1A, the corresponding transitions are shown with more delay since

they are not critical when XFR falling isolates the storage node. The SFBIAS signal

needs to fall only in the case of FIG. 2B; when there is a transfer transistor the bias can be

steady.

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Also shown in FIG. 2B is the signal VSFD1 to illustrate an embodiment of the

present invention in which VSFD1 is pulsed. As disclosed herein, the VSFD1 node may

always be left high, or, as shown in FIG. 2B VSFD1 may be pulsed thus saving power. In

embodiments of the present invention in which VSFD1 is pulsed, terminate will become

10   true during a pulse. VSFD1 is held high until RESET goes high or, in embodiments

employing a transfer transistor, until XFR goes low.

Second MOS N-Channel source-follower transistor 30 is larger than first MOS N-

Channel source-follower transistor 20, and its gate capacitance (the capacitive storage

15   node 26) is therefore correspondingly larger. This provides the advantage of additional

noise immunity for the pixel sensor 10 because more charge needs to be transferred to or

from the capacitive storage node 26 to cause a given voltage change than is the case with

the photocharge integration node 16.

The control signals depicted in FIGS. 2A and 2B may be generated using conventional timing and control logic. To this end, timing and control logic circuit 38 is shown in FIG. 1. The configuration of timing and control logic circuit 38 will depend on

5   the particular embodiment of the present invention, but in any event will be conventional circuitry, the particular design of which is a trivial task for persons of ordinary skill in the art having examined FIGS. 2A and 2B once a particular embodiment of the present invention is selected.

10   Referring again to FIG. 1, an auto-exposure circuit 40 for use with pixel sensors according to a second aspect of the present invention is disclosed. According to this aspect of the invention, each pixel in the array includes a MOS N-Channel saturation level transistor 42, having its source coupled to the output node 22 of the first MOS N-Channel source-follower transistor 20, its gate coupled to SAT. LEVEL line 44, and its

15   drain connected to a global current summing node 46. Global current summing node 46 is coupled to a current comparator 48. Persons of ordinary skill in the art will appreciate that current comparator 48 may comprise a diode load or a resistor coupled between a voltage source and global current summing node 46 driving one input of a voltage

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comparator. The other input of the voltage comparator would be coupled to a voltage

representing a desired number of saturated pixels. Alternatively, an analog-to-digital

converter may be used and the comparison may be done digitally.

5   A saturation level transistor 42 can be used, only if the bias transistor 24 is

present, to divert the bias current from saturated pixel sensors onto a global current

summing line that can be monitored during exposure to determine how many pixels have

reached the saturation level. External circuits can control the threshold for what is

deemed saturation, and can measure the current instead of just comparing it to a

10   threshold, so it is possible through this added transistor and global current summing line

to measure how many pixel sensors have crossed any particular level. Therefore,

by performing rapid variation of the threshold (SAT. LEVEL) and rapid measurement

(e.g. through an A/D converter and input to a processor), it is possible to have access to a

complete cumulative histogram of exposure levels during the exposure; from this

15   information, it is possible to make more complex determinations of good exposure levels,

beyond the simple threshold method used in the presently preferred embodiment.

When the bias transistor 24 is present, isolating the storage node involves timing

signals to turn off both the bias transistor 24 and the first source follower 20. It is

simpler, and potentially advantageous in terms of storage integrity, to include a transfer

transistor 28 that can isolate the storage node under control of a single logic signal. The

5   transfer transistor 28 can also be added to the basic circuit, even without the bias

transistor, for a similar advantage, since even turning off the first source follower

transistor 20 reliably involves coordinating the Reset and VR signals, which is a

complexity that can be eliminated with the transfer transistor 28.

10   In operation, the SAT. LEVEL line 44 is driven to a voltage VSAT corresponding

to a selected photocharge saturation level. Because accumulation of photocharge drives

the output node 22 of the first MOS N-Channel source-follower transistor 20 downward,

MOS N-Channel saturation level transistor 42 is initially turned off because its gate

voltage at VSAT is lower than the voltage at node 16. MOS N-Channel saturation level

15   transistor 42 remains off until accumulation of photocharge at photocharge integration

node 16 has lowered its voltage below VSAT (and that at the source of MOS N-Channel

saturation level transistor 42, common to the output node 22 of the first MOS N-Channel

source-follower transistor 20, to a level one Vt below the voltage VSAT). At this point,

MOS N-Channel saturation level transistor 42 turns on and starts to draw current (less than or equal to the bias current through bias transistor 24) from the global current summing node 46.

5   As will be appreciated by persons of ordinary skill in the art, other pixel sensors in the array will also begin to accumulate enough photocharge to turn on their MOS N-Channel saturation level transistors 42, thus drawing additional current from node 46, and further dropping the voltage on global current summing node 46. As will be appreciated by persons of ordinary skill in the art, comparator 48 may be a voltage comparator having 10   one input coupled to global current summing node 46 and one input coupled to a voltage VTERM chosen to correspond to the voltage on global current summing node 46 when a selected number of pixels are saturating (i.e., have their MOS N-Channel saturation level transistors 42 turned on). When the voltage on global current summing node 46 equals VTERM, the comparator 48 generates a TERMINATE EXPOSURE signal that can be 15   used to terminate the exposure period in one of numerous ways, such as by closing a mechanical shutter or initiating end-of-exposure signals (such as the XFR signal) to control the pixel sensors. The TERMINATE EXPOSURE signal can also be used to quench a strobe flash if desired.

Alternatively, A/D converter 50 may be coupled to global current summing line 46

to convert the voltage representing the global summed current to a digital value that can

be processed by employing a smart auto-exposure algorithm shown at reference numeral

5   52.

The auto-exposure circuit 40 of the present invention may be advantageously

operated in a power saving mode by simultaneously pulsing both the VSFD1 signal to the

drain of the source-follower transistor 20 and one or both of the SF bias signal supplied to

10   the gate of source-follower bias transistor 24 and the SAT. LEVEL signal supplied to the

gate of saturation level transistor 42. In such a mode, the auto-exposure sensing current

flows only when these signals are pulsed, at which time the overexposure sensing is

performed. At other times during photointegration, the overexposure currents from each

pixel do not flow, thus saving power. When this mode of operation is used, the auto-

15   exposure circuit 40 can be advantageously used at higher current levels for better signal-

to-noise ratio.

According to another mode of operating the auto-exposure circuit 40 of the present

invention, the SAT. LEVEL voltage at the gates of all saturation level transistors 42 in an

array can be swept from zero to the maximum level do develop a full cumulative

distribution of the states of all pixels in the array. This mode of operation is most useful

5   when A/D converter 50 is used in the auto-exposure circuit 40. In embodiments of the

present invention employing optional transfer transistor 28, this device should either be

turned off before the ramping of SAT. LEVEL voltage each measurement cycle, or an

extra cycle should be performed with the SAT. LEVEL voltage low in order to store a

signal voltage that is not clipped to the variable SAT. LEVEL voltage. An example of an

10   autoexposure algorithm that could use this cumulative distribution information is one that

would analyze the distribution and classify the scenes as being backlit or not, and set

different values of SAT. LEVEL and i-threshold accordingly, during exposure.

In a typical application of the MOS pixel sensor of the present invention, a

15   plurality of such pixel sensors will be disposed in an array. Referring now to FIG. 3, a

block diagram shows an illustrative 2 by 2 portion of an array of pixel sensors and auto-

exposure apparatus according to the present invention. Persons of ordinary skill in the art

will readily appreciate that the array portion disclosed in FIG. 3 is illustrative only and

that arrays of arbitrary size may be fabricated using the teachings herein.

As would be expected by persons of ordinary skill in the art and as shown in FIG.

5   3, common RESET, BARRIER, SF BIAS, and SAT. LEVEL lines will be provided for

all of the pixel sensors in the array. As presently preferred, a separate VSFD line is

provided for each row in the array, although embodiments of the present invention having

a single VSFD node are also contemplated. The source of each N-Channel MOS row

select transistor in FIG. 1 for each pixel sensor in a column of the array will be coupled to

10   a column line associated with that column and the gate of the N-Channel MOS row select

transistor in FIG. 1 for each pixel sensor in a row of the array will be coupled to a ROW

SELECT line associated with that row.

The 2 by 2 portion 60 of the array in FIG. 3 includes two rows and two columns of

15   MOS active pixel sensors according to the present invention. A first row includes MOS

active pixel sensors 62-1 and 62-2; a second row includes MOS active pixel sensors 62-3

and 62-4. A first column includes MOS active pixel sensors 62-1, 62-3; a second column

includes MOS active pixel sensors 62-2 and 62-4.

A first ROW SELECT line 64-1 is connected to the row-select inputs (RSEL) of

MOS active pixel sensors 62-1 and 62-2. A second ROW SELECT line 64-2 is

connected to the row-select inputs (RSEL) of MOS active pixel sensors 62-3 and 62-4.

5   The first and second ROW SELECT lines may be driven from a row decoder (not shown)

as is well known in the art.

A first COLUMN OUTPUT line 66-1 is connected to the outputs (OUT) of MOS

active pixel sensors 62-1 and 62-3. A second COLUMN OUTPUT line 66-2 is connected

10   to the outputs (OUT) of MOS active pixel sensors 62-2 and 62-4. The first and second

COLUMN OUTPUT lines are coupled to a column readout circuit (not shown) as is well

known in the art.

A global RESET line 68 is connected to the reset (R) inputs of all of the MOS

15   active pixel sensors 62-1 through 62-4. A first VSFD line 70-1 is connected to the VSFD

inputs of the MOS active pixel sensors 62-1 and 62-2 in the first row of the array. A

second VSFD line 70-2 is connected to the VSFD inputs of the MOS active pixel sensors

62-3 and 62-4 in the second row of the array. A global BARRIER line 72 is connected to

the BARRIER inputs of all of the MOS active pixel sensors 62-1 through 62-4. A global

SAT LEVEL line 74 is connected to the SAT LEVEL inputs of all of the MOS active

pixel sensors 62-1 through 62-4. A global XFR line 78 is connected to the XFR inputs of

all of the MOS active pixel sensors 62-1 through 62-4.

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Auto-exposure circuit 80 is coupled to the GLOBAL CURRENT SUMMING

LINE line 82 and generates a TERMINATE EXPOSURE signal on line 84 as described

herein. The TERMINATE EXPOSURE signal on line 84 may be used to terminate the

exposure of the image in a known manner, e.g., by closing a mechanical shutter, or

10   electronically by causing the transition of the signals in FIG. 2 that isolate the storage

node and/or quench a strobe flash.

When the array including 2 by 2 portion 60 is driven by the signals shown in FIG.

2, images may be captured. One particular application of such an array is in a digital

15   camera.

Referring now to FIG. 4, a block diagram of an illustrative digital camera 90

employing an array of MOS active pixel sensors and auto-exposure control according to

the present invention is presented in schematic form. A color-separating prism 92 is

shown mounted inside light-tight housing 94. Lens 96 is fitted to the housing in such a

manner that it projects through the input face 98 of the prism 92, an image which is

thereby split into red, green, and blue images, which are each focussed on one of output

5   faces 100, 102, and 104 of prism 82.

        Attached to the three output faces of prism 92 are three chip-on-board assemblies,

labeled 106R, 106G, and 106B, aligned in such a way that the color-separated images fall

on their active areas in registration. Each chip-on-board assembly includes an imaging

10   array of pixel sensors like that partially depicted in FIG. 3 according to the present

invention. Each of these arrays is attached to its respective prism face. One method for

attaching these arrays to the prism faces is disclosed in co-pending application serial No.

09/302,565, filed April 30, 1999, expressly incorporated herein by reference.

15   Signal connections to the chip-on-board assemblies 106R, 106G, and 106B are

made by way of a ribbon cable 108 which is fitted with three connectors that mate with

connectors on the 3 chip-on-board assemblies. In addition, ribbon cable 98 is attached to

a circuit board 110 by way of connector 112. Circuit board 110 comprises the support

electronics for controlling the reading of image data from the three imaging arrays on the

chip-on-board assemblies 106R, 106G, and 106B mounted on the prism 92 as is

understood by those skilled in the art. Cable 114 carries power into camera 80, and

carries out of the camera signals representative of the image captured through lens 86.

5 Cable 114 exits housing 94 through light-tight fixture 116.

While embodiments and applications of this invention have been shown and

described, it would be apparent to those skilled in the art that many more modifications

than mentioned above are possible without departing from the inventive concepts herein.

10 The invention, therefore, is not to be restricted except in the spirit of the appended claims.